

TRANSMITTAL LETTER TO THE UNITED STATES  
DESIGNATED/ELECTED OFFICE (DO/EO/US)  
CONCERNING A FILING UNDER 35 U.S.C. 371ATTORNEY'S DOCKET NUMBER  
07553.0020U.S. APPLICATION NO.  
(If known, see 37 CFR 1.52)

097807896

INTERNATIONAL APPLICATION NO.

PCT/JP99/05821

INTERNATIONAL FILING DATE

October 22, 1999

PRIORITY DATE CLAIMED

October 22, 1998

TITLE OF INVENTION

PLASMA ETCHING METHOD

APPLICANT(S) FOR DO/EO/US

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Applicant(s) herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c)(2)).
- a. ☐ is attached hereto (required only if not communicated by the International Bureau).
- b. ☒ has been communicated by the International Bureau.
- c. ☐ is not required, as the application was filed with the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371 (c)(2)).
- a. ☒ is attached hereto.
- b. ☐ has been previously submitted under 35 U.S.C. 154 (d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3)).
- a. ☐ are attached hereto (required only if not communicated by the International Bureau).
- b. ☐ have been communicated by the International Bureau.
- c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
- d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☒ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☒ Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A Substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821-1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154 (d)(4).
19. ☐ A second copy of the English language translation of the international application 35 U.S.C. 154 (d)(4).
20. ☒ Other items or information:
- a. ☒ Copy of cover page of International Publication No. WO 00/24046
- b. ☐ Copy of Notification of Missing Requirements.
- c. ☐

**Figure 6.** The effect of the initial concentration of the monomer on the polymerization of **1**. Polymerization conditions were as described in Figure 1.

**SPECIFICATION****PLASMA ETCHING METHOD****TECHNICAL FIELD**

The present invention relates to a plasma etching method.

**BACKGROUND ART**

There is a plasma etching device proposed in the prior art, having an upper electrode and a lower electrode provided facing opposite each other inside an air-tight processing chamber. In this device, after placing a workpiece such as a semiconductor wafer (hereafter referred to as a "wafer") on the lower electrode, the processing gas is introduced into the processing chamber and also, vacuum drawing is implemented inside the processing chamber to maintain the atmosphere within at a specific pressure. Next, plasma generating power is applied to the upper electrode and biasing power sustaining a specific power level is applied to the lower electrode. As a result, the processing gas inside the processing chamber becomes dissociated to generate plasma and radicals, and an insulating film such as an  $\text{SiO}_2$  (silicon oxide) film formed on the wafer becomes etched through ion-assist etching by the radicals and the ions in the plasma drawn into the wafer by the biasing power, thereby forming contact holes at the insulating film.

However, when forming contact holes in conformance to the  $0.15\mu\text{m}$  design rule, a higher aspect ratio must be achieved and thus, the etching rate at the insulating film is lowered. In addition, the photoresist film formed at the surface of the insulating film is constantly sputtered with the ions. During this process, the corners formed between the upper surface of the photoresist film and the pattern formation surface tend to be sputtered to a great degree. Consequently, the pattern width of the photoresist film 206 increases as shown in FIG. 2(d), presenting a problem in that a desired contact

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hole 210 cannot be formed. Accordingly, it is essential to achieve a technology that increases the ratio of the etching rate (or the etching quantity) at the insulating film 202 relative to the etching rate (or the etching quantity) at the photoresist film 206 (hereafter referred to as the "selectivity").

An object of the present invention, which has been completed by addressing the problem of the prior art discussed above, is to provide a new and improved plasma etching method that improves the etching selectivity and enables an ultra-fine etching process to be implemented on a workpiece.

#### **DISCLOSURE OF THE INVENTION**

In order to achieve the object described above, in a first aspect of the present invention, a plasma etching method for implementing a specific etching process on a workpiece placed on an electrode provided within a processing chamber by introducing a processing gas into the processing chamber, generating plasma inside the processing chamber with a plasma source and applying biasing power to the electrode, which is characterized in that an etching step in which the workpiece is etched over a specific length of etching time by applying the biasing power to the electrode and a film formation step in which a protective film is formed as an etching mask at a surface of the workpiece over a specific length of film formation time while the biasing power is cut off are sequentially repeated, with the lengths of the individual etching times and the individual film formation times adjusted as the etching process progresses, is provided.

In a second aspect of the present invention, a plasma etching method for implementing a specific etching process on a workpiece placed on an electrode provided within a processing chamber by introducing a processing gas into the processing chamber, generating

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plasma inside the processing chamber with a plasma source and applying biasing power to the electrode, which is characterized in that an etching step in which a workpiece is etched over a specific length of etching time by applying the biasing power to the electrode and a film formation step in which a protective film is formed as an etching mask at a surface of the workpiece over a specific length of film formation time while the biasing power is cut off are sequentially repeated, with the process starting with the film formation step and ending with the etching step is provided.

Adopting such an etching method, in which the etching process is implemented by repetitively performing the etching step and the film formation step, makes it possible to etch the workpiece while protecting the etching mask such as a photoresist film with the protective film. As a result, since the photoresist film is not readily etched and higher selectivity is achieved, the pattern at the photoresist film is prevented from spreading. In addition, since the protective film is formed at the mask pattern sidewalls during the film formation step, desired contact holes can be formed at the workpiece.

By adjusting the lengths of the individual etching times and the individual film formation times as the etching process progresses, a desired etching process can be implemented even if the states of the workpiece and the photoresist film change during the process.

Furthermore, the lengths of the individual film formation times may be extended as the etching process progresses. As the process progresses, the aspect ratio of the contact holes increases, which makes it difficult to form a protective film at the bottom surfaces of the contact holes. Thus, by extending the lengths of the individual film formation times, it is possible to ensure that the photoresist film is protected with a higher degree of reliability while implementing a specific etching process.

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In addition, by setting the lengths of the individual film formation times at one second or longer, the protective film can be formed at the photoresist film with a high degree of reliability during the film formation steps.

By implementing an etching step at the end of the etching process, the protective film formed at the bottom surfaces of the contact holes and the photoresist film can be removed, thereby eliminating the need to implement a step for removing the protective film to allow the post-process to be completed promptly.

Furthermore, by implementing a film formation step at the beginning of the etching process, the photoresist film becomes protected by the protective film prior to the etching step, thereby enabling a desired process to be implemented on the workpiece.

Moreover, by constituting the etching target with a silicon oxide film and using a gas containing fluorocarbon gas as the processing gas, a protective film can be formed at the photoresist with a high degree of reliability and desired contact holes can be formed at the SiO<sub>2</sub> film.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

FIG. 1 is a schematic sectional view of an etching device in which the present invention may be adopted;

FIG. 2 presents schematic sectional views of a wafer W, illustrating the etching method adopted in the etching device shown in FIG. 1 and an etching method in the prior art;

FIG. 3 schematically illustrates the relationship between the selectivity and the duty to facilitate an explanation of the etching method adopted in the etching device shown in FIG. 1;

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FIG. 4 schematically illustrates the on/off cycle of the biasing power to facilitate the explanation of the etching method adopted in the etching device shown in FIG. 1;

FIG. 5 schematically illustrates the relationship between the length of the entire process time and the etching rate at the insulating film observed as the duty is varied to facilitate the explanation of the etching method adopted in the etching device shown in FIG. 1;

FIG. 6 schematically illustrates the relationship between the thickness of the remaining photoresist film and the duty to facilitate the explanation of the etching method adopted in the etching device shown in FIG. 1;

FIG. 7 presents schematic sectional views of the wafer W, illustrating the etching method adopted in the etching device shown in FIG. 1;

FIG. 8 schematically illustrates the relationship between the aspect ratio and the thickness of the polymer to facilitate the explanation of the etching method adopted in the etching device shown in FIG. 1; and

FIG. 9 schematically illustrates the relationship between the biasing power off time and the thickness of the polymer to facilitate the explanation of the etching method adopted in the etching device shown in FIG. 1.

## **THE BEST MODE FOR CARRYING OUT THE INVENTION**

The following is an explanation of an embodiment of the plasma etching method according to the present invention, given in reference to the attached drawings.

(1) Overall structure of etching device

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First, in reference to FIG. 1, the overall structure of a plane parallel type plasma etching device 100 in which the present invention may be adopted is explained.

A processing chamber 102 of the etching device 100 is formed inside an electrically conductive processing container 104 which is grounded for safety. Inside the processing chamber 102, a conductive lower electrode 106 is provided. The lower electrode 106 also functions as a stage on which a wafer W is placed. In addition a biasing power supply 110 that outputs biasing power in the embodiment is connected to the lower electrode 106 via a matcher 108. A controller 112 that controls the supply of biasing power is connected to the biasing power supply 110. It is to be noted that the structure adopted to implement the biasing power control is to be detailed later.

In addition, a conductive upper electrode 114 is provided at a position facing opposite the mounting surface of the lower electrode 106. Between the upper electrode 114 and the processing container 104, an insulating member 116 is provided. A plasma generating power supply 120 that outputs plasma generating power, the frequency of which is high relative to the frequency of the biasing power, is connected to the upper electrode 114 via a matcher 118. The controller 112 is also connected to the plasma generating source 120, to control the supply of plasma generating power.

Numerous gas outlet holes 114a are formed at the upper electrode 114. A processing gas supplied from a processing gas supply source (not shown) is evenly supplied into the processing container 104 via a gas supply pipe 122 and the gas supply holes 114a. Furthermore, an evacuating pipe 124 is connected at a lower position inside the processing container 104, with a vacuum pump (not shown) connected to the evacuating pipe 124.

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## (2) Etching process steps

Next, the etching process steps in performed the embodiment are explained in detail in reference to FIGS. 1 ~ 9.

First, the wafer W is placed on the lower electrode 106 in FIG. 1. At the wafer W, an insulating film 202 constituted of, for instance,  $\text{SiO}_2$  is formed on a substrate 200 constituting the wafer W and a photoresist film 206 having a specific pattern 204 formed therein and constituting an etching mask is laminated over the insulating film 202 as illustrated in FIG. 2(a). In addition, the processing gas constituted of a mixed gas containing, for instance,  $\text{C}_4\text{F}_8$ , CO, Ar and  $\text{O}_2$  is introduced into the processing chamber 102 in FIG. 1 from the gas supply source via the gas supply pipe 122 and the gas outlet holes 114a. At this time, the flow rates of  $\text{C}_4\text{F}_8$ , CO, Ar and  $\text{O}_2$  are set to achieve a flow rate ratio of 1:4:15:1. Vacuum drawing is implemented inside the processing chamber 102 via the evacuating pipe 124 to sustain the pressure of the atmosphere at, for instance, 35mTorr.

Next, the controller 112 implements control to apply a high-frequency power with a frequency of 27 MHz and a power level of 4 W ~ 5 W per  $\text{cm}^2$  of the upper electrode (114) to the upper electrode 114 from the plasma generating power supply 120 via the matcher 118 and, as described later, to intermittently apply a high-frequency power with a relatively low frequency of 800 KHz compared to the frequency of the plasma generating power and a power level of 5 W per  $\text{cm}^2$  of the wafer W to the lower electrode 106 from the biasing power supply 110 via the matcher 108.

Now, in reference to FIGS. 2 ~ 9, the structure adopted to implement the biasing power control is explained.

As illustrated in FIG. 4, on-cycle processing (hereafter referred to as an "etching step") during which the biasing power is applied is first implemented. Next, off-cycle processing (hereafter referred to as a

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"film formation step") during which the biasing power is not applied is implemented. FIG. 3 illustrates the relationship between the selectivity and the duty at a given position on the wafer W at a point in time at which nine etching steps and eight film formation steps have been alternately performed. The selectivity represents a ratio; quantity of insulating film 202 that has been etched/quantity of photoresist film 206 that has been etched. The duty represents; on-cycle period / ( on-cycle period + off-cycle period). In addition, the on-cycle period is set at 30 seconds whereas the off cycle period is set at a length of time that achieves the duty. It is to be noted that the duty of 100% is achieved when the biasing power is continuously applied. It is not always necessary to cut off the biasing power during the film formation step and the biasing power may be reduced to a degree at which a film can be formed, instead.

FIG. 3 shows that by lowering the duty, the selectivity can be improved. One conceivable reason for this is as follows. While the biasing power is applied to the lower electrode 106 (during an etching step), the insulating film 202 becomes etched through ion-assist etching by CF<sub>x</sub> ions and CF<sub>x</sub> radicals generated through the dissociation of C<sub>4</sub>F<sub>8</sub>, Ar ions and the like. The photoresist film 206, on the other hand, is sputtered (etched) by the ions at an etching rate lower than that at the insulating film 202.

When the biasing power is not applied (during a film formation step), ions are not drawn to the wafer W. As a result, as shown in FIG. 2(b), the CF<sub>x</sub> radicals becoming adhered to a surface of the photoresist film 206 form a polymer film 208. Likewise, a polymer film 208 is formed at a surface of the insulating film 202 as well. However, since the surface of the insulating film 202 is set deeper by, at least, a degree corresponding to the thickness of the photoresist film 206 and the radical particles undergo thermal motion (random motion), the

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thickness (B) of the polymer formed at the surface of the insulating film 202 is smaller than the thickness (A) of the polymer film 208 formed at the surface of the photoresist film 206. This point will be detailed later in reference to FIG. 8.

Furthermore, the polymer film 208 can be assumed to adhere more readily to the photoresist film 206 which is constituted of all, for instance,  $CxFyOz$  and is closer to the polymer film 208 in molecular composition than the insulating film 202 constituted of  $SiO_2$ . This point will be detailed later in reference to FIG. 9.

During an etching step implemented after the film formation step, the polymer film 208 functions as a protective film for the photoresist film 206. Namely, since the polymer film 208 is first etched and then the photoresist film 206 is etched, the quantity of the photoresist film 206 that is etched is reduced. Since the thickness of the polymer film 208 on the insulating film 202 is small, the progress of the etching process on the insulating film 202 is not greatly hindered.

During an etching step, the insulating film 202 is etched at an etching rate of approximately 8000 angstroms /min, the photoresist film 206 is etched at an etching rate of approximately 800 angstroms /min and the polymer film 208 constituting the protective film is etched at an etching rate of approximately 2300 angstroms/min. During the film formation step, the polymer film 208 is formed at the surface of the photoresist film 206 at approximately 1800 angstroms/min. This substantiates the selectivity of 10 achieved by constantly applying biasing power and a selectivity of 15 achieved when the biasing power is applied at a duty of 50% as shown in FIG. 3.

In addition, FIG. 5 illustrates the relationship between the entire length of the process time and the average etching rate (etching

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quantity at the insulating film 202/entire length of time for the process including film formation steps) at the insulating film 202 observed by varying the duty under conditions identical to those in FIG. 3. FIG. 5 indicates that when the duty is lowered, the average etching rate is reduced and the entire length of time for the process increases.

FIG. 6 shows the thickness of the photoresist film 206 remaining unetched when the entire process is completed by changing the duty under conditions identical to those in FIG. 3. FIG. 6 indicates that by lowering the duty, the quantity of the remaining photoresist film 206 is increased to enable formation of a contact hole 210 (see FIG. 2(c)) having the desired shape as a result.

FIG. 7(b) illustrates the states of the bottom surface of the contact hole 210 and the polymer 218 formed at the upper surface of the photoresist film 206 after a film formation step is implemented over a specific length of time on the wafer W shown in FIG. 7(a). In addition, FIG. 8 indicates the ratio of the thickness B of the polymer film 208 formed at the bottom surface of the contact hole 210 relative to the thickness A of the polymer film 208 formed at the upper surface of the photoresist film 206, achieved by varying the aspect ratio of the contact hole 210 shown in FIG. 7(b). It is to be noted that in this specification, the aspect ratio refers to the ratio ( $d/r$ ) of the distance  $d$  between the upper surface of the photoresist film 206 and the bottom surface of the insulating film 202 and the diameter  $r$  of the contact hole 210.

FIG. 8 indicates that as the aspect ratio increases, i.e., as the etching process progresses to deepen the contact hole 210, the thickness B of the polymer film 208 formed at the bottom surface of the 210 becomes smaller relative to the thickness A of the polymer film 208 formed at the upper surface of the photoresist film 206.

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FIG. 9 presents a comparison of the speed at which the film constituted of the polymer film 208 is formed when the photoresist film 206 is formed at the surface of the wafer W and the speed at which the film constituted of the polymer film 208 is formed when the insulating film ( $\text{SiO}_2$  film) 202 is formed at the surface of the wafer W, during a film formation step implemented under process conditions identical to those in FIG. 3. FIG. 9 indicates that no polymer film 208 is formed on the insulating film 202 until the polymer film 208 is formed on the photoresist film 206 at approximately 120 angstroms. During such a short period of time (5 seconds), the polymer film 208 or the like is not formed at the insulating film 202 even if the application of the biasing power is stopped.

The following conclusion may be drawn from the test data discussed above. FIG. 4 shows a process starting with an etching step and ending with an etching step with each etching step extending over 30 seconds, as explained earlier. If an etching step is implemented at the beginning and at the end of the process in this manner, the entire length of time for the process can be reduced by increasing the length of time corresponding to a single cycle constituted of an etching step and a film formation step even when the duty remains unchanged.

In addition, an etching step is implemented at the end of the process in the embodiment, since residues such as the polymer film 208 would remain adhering to the surface of the photoresist film 206 and the bottom surface of the contact hole 210 if a film formation step was implemented at the end of the process to necessitate a step removing the polymer and the like to be implemented resulting in a reduction in the throughput. In other words, during an etching step at the end of the process, etching is performed until the polymer film 208 is removed and the formation of the contact hole 210 is completed.

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Moreover, as shown in FIG. 9, if the film formation step is implemented for only five seconds, no polymer film 208 is formed on the insulating film 202 while a polymer film 208 is formed on the photoresist film 206. While the length of time may be other than five seconds depending upon the process conditions such as the type of processing gas being used, the polymer film 208 is formed on the photoresist film 206 as long as the film formation step is implemented over at least one second to achieve an advantage similar to that described above. It is to be noted that generally, the length of time for the etching step should be set greater than the length of time the film formation step to reduce the process time. In addition, since the on/off cycle of the biasing power is one second or longer in the embodiment, easy on / off control on the power supply is achieved in the software without having to utilize a special pulse source.

When the diameter of the contact hole 210 is small, a specific aspect ratio is assured at the beginning of the etching process. Thus, as shown in FIG. 8, since the polymer film 208 is formed at a very small thickness on the insulating film 202 even if a film formation step is implemented at the beginning of the process, the etching speed is not greatly reduced and, at the same time, the polymer film 208 is formed at the photoresist film 206 in advance to achieve an improvement in the selectivity.

Moreover, as the etching process progresses, the aspect ratio of the contact hole 210 increases and the speed at which the film constituted of the polymer film 208 is formed at the bottom surface of the contact hole 210 during the film formation step becomes lowered. As a result, the degree to which the contact hole 210 is prevented from becoming etched by implementing the film formation step is reduced compared to that at the beginning of the etching process. Consequently, by lowering the duty or reducing the length of time for

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the etching step, increasing the length of time for the film formation step as the etching process progresses, a specific etching process can be implemented on the insulating film 202 while forming the polymer film 208 at the photoresist film 206 with a high degree of reliability.

In addition, by adopting the embodiment, in which the photoresist film 206 is etched after the polymer film 208 formed on the photoresist film 206 through the film formation step, the selectivity can be raised. It is to be noted, however, that if the selectivity is raised to an excessive degree, the length of the process time increases.

Only a small quantity of the photoresist film 206 needs to remain unetched, which is enough to ensure that the contact hole 10 with a poor shape shown in FIG. 2(d) is not formed when the entire process is completed. Accordingly, the duty and the lengths of time for a single etching step and a single film formation step are set so as to minimize the length of time for the process by taking into consideration factors such as the thicknesses of the insulating film 202 and the photoresist film 206, the etching rates at the insulating film 202 and at the photoresist film 206, the film formation rate for the polymer film 208, the diameter of the contact holes being formed, the degree to which the etching process progresses, the type of processing gas being used, the level of the biasing power and the like.

In the embodiment implemented as described above in which the etching process is performed while forming the polymer film 208 at the upper surface and the shoulders of the photoresist film 206, the photoresist film 206 is not etched to an excessive degree during the process and, in particular, shoulders 206a in FIG. 2(c) are protected from damage. As a result, a contact hole 210 achieving a high aspect ratio can be formed with a high degree of reliability based upon the pattern 204. In addition, since the polymer film 208

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becomes adhered to the inner side surface of the contact hole 210 as shown in FIG. 2(b), the inner sidewall of the contact hole 210 that has already been formed is not readily etched, thereby effectively preventing the contact hole 210 from becoming bowed.

While the invention has been particularly shown and described with respect to the preferred embodiment thereof by referring to the attached drawings, the present invention is not limited to this example and it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit, scope and teaching of the invention.

For instance, while an explanation is given in reference to the embodiment on an example in which biasing power at 800 KHz is applied to the lower electrode, the present invention may be implemented by applying power with a frequency other than 800 KHz as the biasing power.

Furthermore, while an explanation is given in reference to the embodiment on an example in which the insulating film is constituted of  $\text{SiO}_2$ , the present invention is not limited to this example and it may be adopted to etch an insulating film constituted of, for instance, BPSG (boron-phospho-silicate glass), TEOS (tetra-ethylorth-osilicate), SOG (spin-on glass),  $\text{SiOF}$  or a thermal oxide film ( $\text{SiO}_2$ ) or to implement an etching process on a target other than an insulating film.

Moreover, while an explanation is given in reference to the embodiment on an example in which the present invention is adopted in conjunction with a plane parallel type plasma etching device, the present invention is not limited to this example and it may be adopted in a plasma etching device having a plasma source such as an inductively coupled etching device or a microwave etching device as long as biasing power can be applied to the workpiece.

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## INDUSTRIAL APPLICABILITY

The present invention may be adopted in a plasma etching method. In particular, the present invention is ideal in application requiring a high aspect ratio such as ultra-fine processing to be implemented in conformance to the 0.15 $\mu$ m design rules.

**WHAT IS CLAIMED IS;**

1. A plasma etching method for implementing a specific etching process on a workpiece placed on an electrode provided within a processing chamber by introducing a processing gas into said processing chamber, generating plasma inside said processing chamber with a plasma source and applying biasing power to said electrode, wherein;

an etching step in which the workpiece is etched over a specific length of etching time by applying the biasing power to said electrode and a film formation step in which a protective film is formed as an etching mask at a surface of the workpiece over a specific length of film formation time while the biasing power is cut off are sequentially repeated, with the lengths of individual etching times and individual film formation times adjusted as the etching process progresses.

2. A plasma etching method according to claim 1, wherein:

the lengths of the film formation times are extended relative to the extent to which the etching process has progressed.

3. A plasma etching method according to claim 1, wherein:

the lengths of the film formation times are set at 1 second or longer.

4. A plasma etching method according to claim 1, wherein:

said etching step is implemented as a final step of said etching process.

5. A plasma etching method according to claim 1, wherein:

said film formation step is implemented as a first step of said etching process.

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6. A plasma etching method according to claim 1, wherein:  
the etching target is a silicon oxide film; and  
said processing gas is constituted of a gas containing fluorocarbon gas.

7. A plasma etching method for implementing a specific etching process on a workpiece placed on an electrode provided within a processing chamber by introducing a processing gas into said processing chamber, generating plasma inside said processing chamber with a plasma source and applying biasing power to said electrode, wherein;

an etching step in which the workpiece is etched over a specific length of etching time by applying the biasing power to said electrode and a film formation step in which a protective film is formed as an etching mask at a surface of the workpiece over a specific length of film formation time while the biasing power is cut off are sequentially repeated, with the process starting with said film formation step and ending with said etching step.

8. A plasma etching method according to claim 7, wherein;  
the lengths of individual etching times and individual film formation times are adjusted as said etching process progresses.

9. A plasma etching method according to claim 7, wherein:  
the lengths of individual film formation times are extended relative to the extent to which said etching process progresses.

10. A plasma etching method according to claim 7, wherein:

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the lengths of individual film formation times are set at 1 second or longer.

11. A plasma etching method according to claim 7, wherein:

the etching target is a silicon oxide film; and

said processing gas is constituted of a gas containing fluorocarbon gas.

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**ABSTRACT OF THE DISCLOSURE**

A wafer W is placed on a lower electrode 106 provided inside a processing chamber 102 of an etching apparatus 100 and a gas containing C4F8 is induced into the processing chamber 102. A controller 112 implements control to apply 27MHz power to an upper electrode 114 from a plasma generating power supply 120 and to intermittently apply 800KHz power to the lower electrode 106 from a biasing power supply 108. While the biasing power is on, an insulating film 202 constituted of SiO2 at the wafer W is etched, whereas a polymer (protective film) 208 is formed at a photoresist film 206 while the biasing power is off. Adopting the above method, contact holes achieving a specific shape can be formed by improving the selectivity of the insulating film relative to the photoresist film.

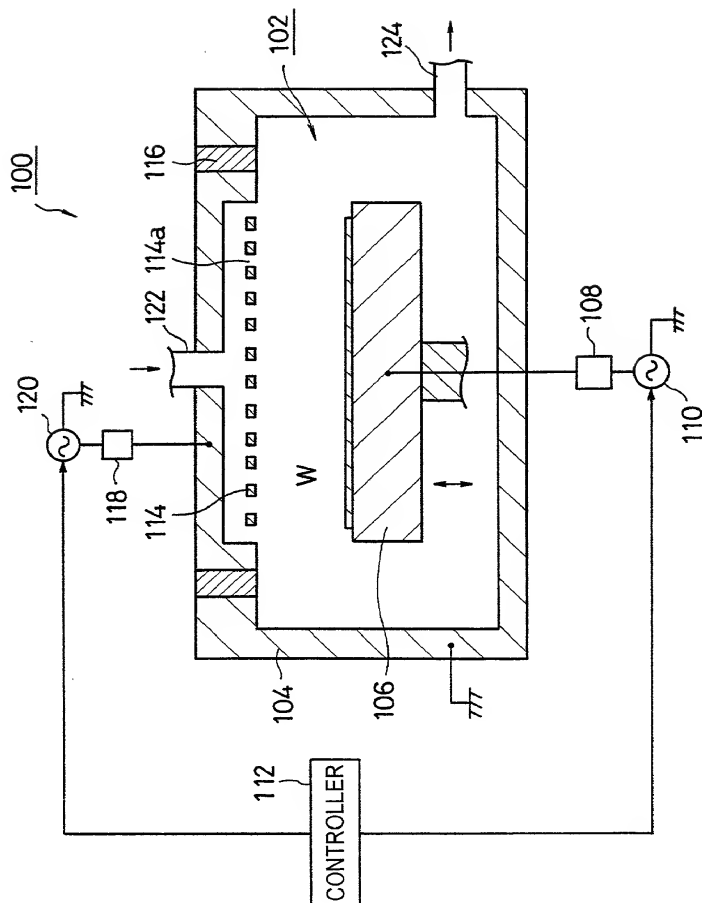
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**EXPLANATION OF THE REFERENCE NUMERALS**

100 etching device  
102 processing chamber  
104 processing container  
106 lower electrode  
108 matcher  
110 biasing power supply  
121 controller  
114 upper electrode  
114a gas outlet hole  
116 insulating member  
118 matcher  
120 plasma generating power supply  
122 gas supply pipe  
124 evacuating pipe  
200 substrate  
202 insulating film  
206 photoresist film  
208 polymer (protective film)  
210 contact hole  
W wafer

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FIG.1



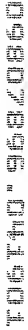
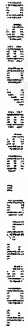
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FIG.2(c)

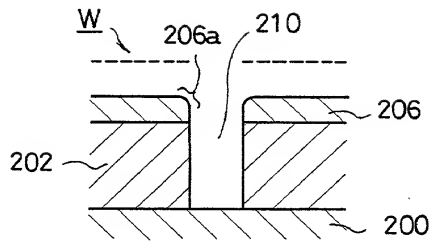


FIG.2(d)

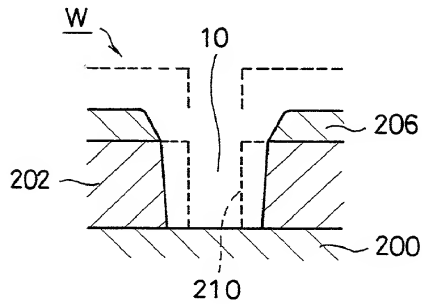
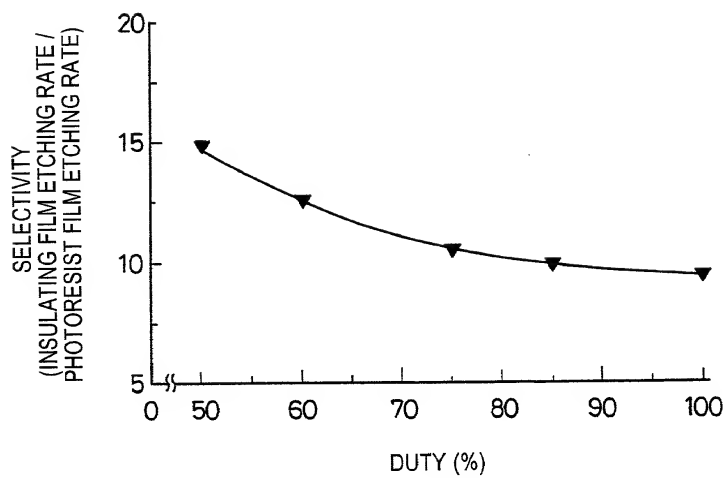
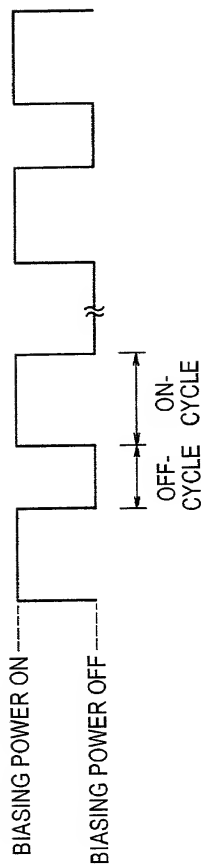


FIG.3



5/10

FIG.4



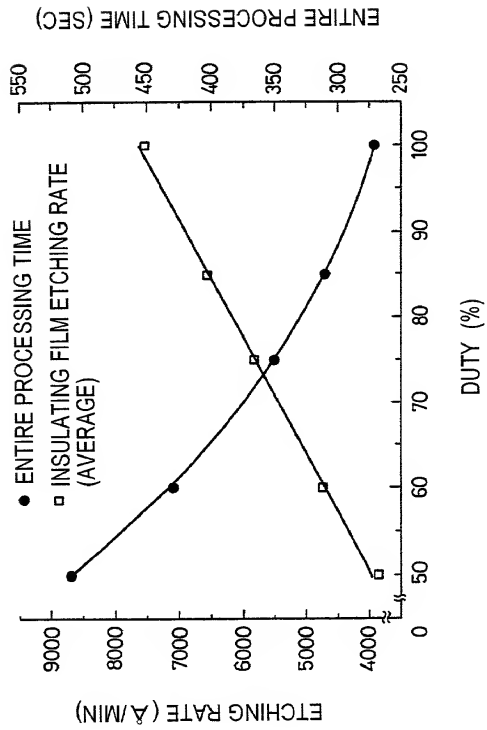


FIG.5

FIG.6

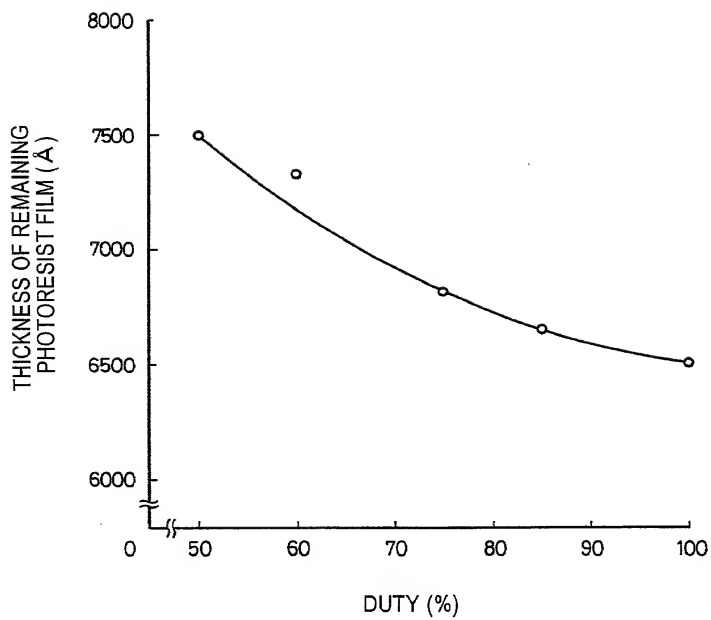


FIG.7(a)

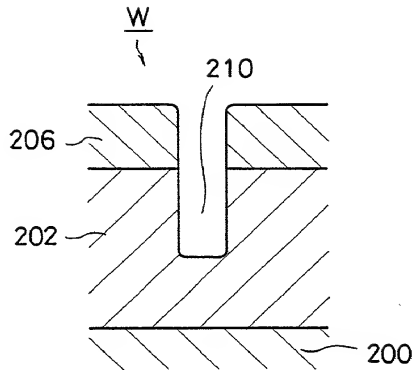


FIG.7(b)

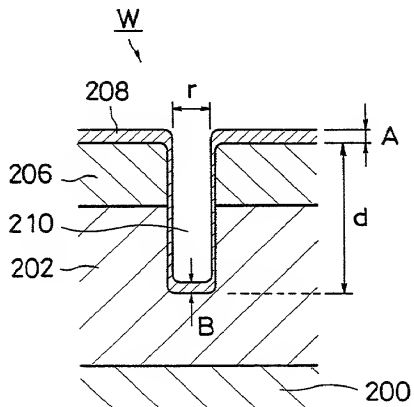


FIG.8

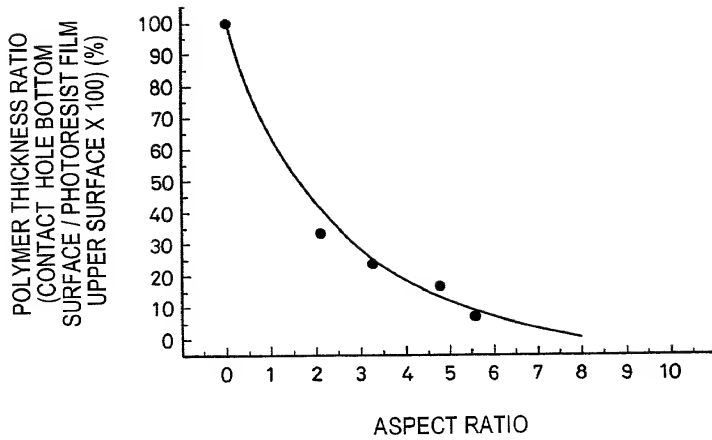
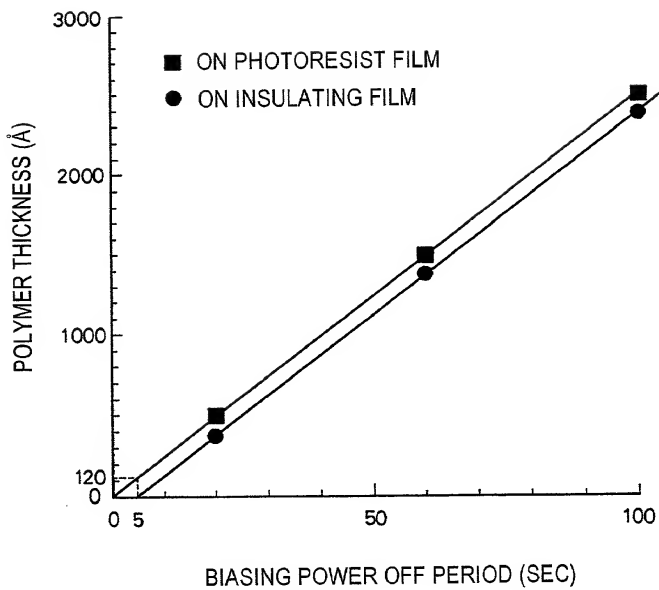


FIG.9





## DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: PLASMA ETCHING METHOD

the specification of which ☐ is attached and/or ☒ was filed on October 22, 1999 as United States Application Serial No. \_\_\_\_\_ or PCT International Application No. PCT/JP99/05821 and was amended on January 19, 2000 (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT International application(s) designating at least one country other than the United States, listed below and have also identified below, any foreign application(s) for patent or inventor's certificate, or any PCT International application(s) having a filing date before that of the application(s) of which priority is claimed:

Country	Application Number	Date of Filing	Priority Claimed Under 35 U.S.C.
Japan	JP10-319942	October 22, 1998	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO
PCT	PCT/JP99/05821	October 22, 1999	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

Application Number	Date of Filing

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) or § 365(c) of any PCT International application(s) designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application(s) and the national or PCT International filing date of this application:

Application Number	Date of Filing	Status (Patented, Pending, Abandoned)

I hereby appoint the following attorney and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P., Douglas B. Henderson, Reg. No. 20,291; Ford F. Farabow, Jr., Reg. No. 20,630; Arthur S. Garrett, Reg. No. 20,338; Donald R. Dunner, Reg. No. 19,073; Brian G. Brunsvold, Reg. No. 22,593; Tipton D. Jennings, IV, Reg. No. 20,645; Jerry D. Voight, Reg. No. 23,020; Laurence R. Hefter, Reg. No. 20,827; Kenneth E. Payne, Reg. No. 23,098; Herbert H. Mintz, Reg. No. 24,691; C. Larry O'Rourke, Reg. No. 26,014; Albert J. Santorelli, Reg. No. 22,610; Michael C. Elmer, Reg. No. 25,857; Richard H. Smith, Reg. No. 20,609; Stephen L. Peterson, Reg. No. 26,325; John M. Romary, Reg. No. 26,331; Bruce C. Zotter, Reg. No. 27,680; Dennis P. O'Reilly, Reg. No. 27,932; Allen M. Sokal, Reg. No. 26,695; Robert D. Bajefsky, Reg. No. 25,387; Richard L. Stroup, Reg. No. 28,478; David W. Hill, Reg. No. 28,220; Thomas L. Irving, Reg. No. 28,619; Charles E. Lipsey, Reg. No. 28,165; Thomas W. Winland, Reg. No. 27,605; Basil J. Lewis, Reg. No. 28,818; Martin I. Fuchs, Reg. No. 28,508; E. Robert Yoches, Reg. No. 30,120; Barry W. Graham, Reg. No. 29,924; Susan Haberman Griffen, Reg. No. 30,907; Richard B. Racine, Reg. No. 30,415; Thomas H. Jenkins, Reg. No. 30,857; Robert E. Converse, Jr., Reg. No. 27,432; Clair X. Mullen, Jr., Reg. No. 20,348; Christopher P. Foley, Reg. No. 31,354; John C. Paul, Reg. No. 30,413; Roger D. Taylor, Reg. No. 28,992; David M. Kelly, Reg. No. 30,953; Kenneth J. Meyers, Reg. No. 25,146; Carol P. Elnaudi, Reg. No. 32,220; Walter Y. Boyd, Jr., Reg. No. 31,738; Steven M. Anzalone, Reg. No. 32,095; Jean B. Fordis, Reg. No. 32,984; Barbara C. McCurdy, Reg. No. 32,120; James K. Hammond, Reg. No. 31,964; Richard V. Burguljan, Reg. No. 31,744; J. Michael Jakes, Reg. No. 32,824; Thomas W. Banks, Reg. No. 32,719; Christopher P. Isaac, Reg. No. 32,616; Bryan C. Diner, Reg. No. 32,409; M. Paul Barker, Reg. No. 32,013; Andrew Chanho Sonu, Reg. No. 33,457; David S. Forman, Reg. No. 33,694; Vincent P. Kovalick, Reg. No. 32,867; James W. Edmondson, Reg. No. 33,871; Michael R. McGurk, Reg. No. 32,045; Joann M. Neth, Reg. No. 36,363; Gerson S. Panitch, Reg. No. 33,751; Cheryl M. Taylor, Reg. No. 33,216; Charles E. Van Horn, Reg. No. 40,266; Linda A. Wadler, Reg. No. 33,218; Jeffrey A. Berkowitz, Reg. No. 36,743; Michael R. Kelly, Reg. No. 33,921; James B. Monroe, Reg. No. 33,971; Doris Johnson Hines, Reg. No. 34,629; Allen R. Jensen, Reg. No. 28,274; Lori Ann Johnson, Reg. No. 34,428; and David A. Manspeizer, Reg. No. 37,540 and \_\_\_\_\_ Please address all correspondence to FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P., 1300 I Street, N.W., Washington, D.C. 20005, Telephone No. (202) 408-4000.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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Residence				Citizenship	
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